WHAT IS CLAIMED IS:

1. A power semiconductor device comprising:

a base layer of a first conductivity type;

a base layer of a second conductivity type selectively formed on one surface of said base layer of the first conductivity type;

one of an emitter layer and source layer of the first conductivity type selectively formed on the surface of said base layer of the second conductivity type;

one of a collector layer and drain layer selectively formed on one of the one surface and the other surface of said base layer of the first conductivity type;

a first main electrode formed on said one of said collector layer and drain layer;

a second main electrode formed on said one of said emitter layer and source layer of the first conductivity type and on said base layer of the second conductivity type; and

a gate electrode formed above part of said base layer of the second conductivity type which lies between said one of said emitter layer and source layer of the first conductivity type and said base layer of the first conductivity type with first and second gate insulating films disposed therebetween;

wherein capacitance of a capacitor formed of the

second gate insulating film is different from that of a capacitor formed of the first gate insulating film.

2. The power semiconductor device according to claim 1, wherein the first gate insulating film is formed in a portion near said one of said emitter layer and source layer of the first conductivity type and the second gate insulating film is formed in a portion near said base layer of the first conductivity type.

3. The power semiconductor device according to claim 2, wherein thickness of the second gate insulating film is larger than that of the first gate insulating film.

4. The power semiconductor device according to claim 2, wherein a dielectric constant of the second gate insulating film is smaller than that of the first gate insulating film.

5. The power semiconductor device according to claim 2, wherein thickness of the second gate insulating film has an inclination and the thickness thereof on the side of said one of said emitter layer and source layer of the first conductivity type is smaller than that on the side of said base layer of the first conductivity type.

6. The power semiconductor device according to claim 1, wherein said gate electrode is buried in a trench with the first and second gate insulating films disposed therebetween to form a trench structure,

the trench being formed to range from the surface of said one of said emitter layer and source layer of the first conductivity type to an intermediate portion of said base layer of the first conductivity type via said base layer of the second conductivity type.

7. The power semiconductor device according to claim 2, wherein said gate electrode is buried in a trench with the first and second gate insulating films disposed therebetween to form a trench structure, the trench being formed to range from the surface of said one of the emitter layer and source layer of the first conductivity type to an intermediate portion of said base layer of the first conductivity type via said base layer of the second conductivity type.

8. The power semiconductor device according to claim 3, wherein said gate electrode is buried in a trench with the first and second gate insulating films disposed therebetween to form a trench structure, the trench being formed to range from the surface of said one of the emitter layer and source layer of the first conductivity type to an intermediate portion of said base layer of the first conductivity type via said base layer of the second conductivity type.

9. The power semiconductor device according to claim 4, wherein said gate electrode is buried in a trench with the first and second gate insulating films disposed therebetween to form a trench structure,

the trench being formed to range from the surface of said one of the emitter layer and source layer of the first conductivity type to an intermediate portion of said base layer of the first conductivity type via said base layer of the second conductivity type.

10. The power semiconductor device according to claim 5, wherein said gate electrode is buried in a trench with the first and second gate insulating films disposed therebetween to form a trench structure, the trench being formed to range from the surface of said one of the emitter layer and source layer of the first conductivity type to an intermediate portion of said base layer of the first conductivity type via said base layer of the second conductivity type.

11. A manufacturing method of a power semiconductor device comprising:

forming a base layer of a first conductivity type;

selectively forming a base layer of a second conductivity type on one surface of the base layer of the first conductivity type;

selectively forming one of an emitter layer and source layer of the first conductivity type on the surface of the base layer of the second conductivity type;

selectively forming one of a collector layer and drain layer on one of the one surface and the other surface of the base layer of the first conductivity

type;

forming a first main electrode on said one of the collector layer and drain layer;

forming a second main electrode on said one of the emitter layer and source layer of the first conductivity type and on the base layer of the second conductivity type; and

forming first and second gate insulating films on part of the base layer of the second conductivity type which lies between said one of the emitter layer and source layer of the first conductivity type and the base layer of the first conductivity type and forming a gate electrode on the first and second gate insulating films;

wherein capacitance of a capacitor formed of the second gate insulating film is different from that of a capacitor formed of the first gate insulating film.

add A7

add B7